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Development of Enhanced Avionics Flight Hardware Selection Process

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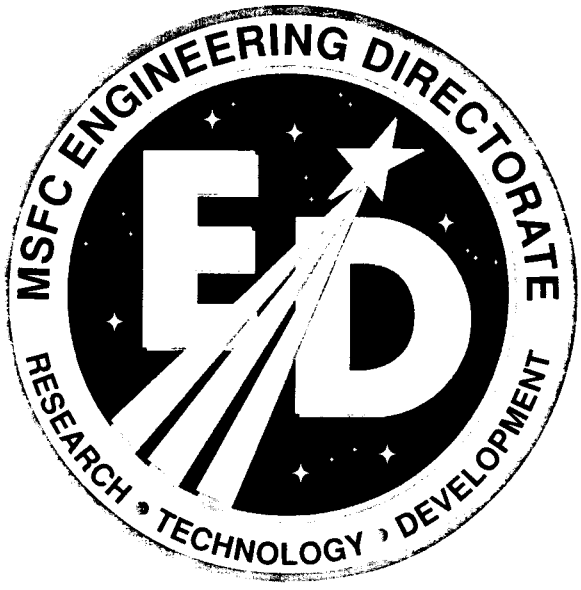

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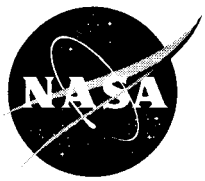

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National Aeronautics and
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LIST OF ACRONYMS

A/D	analog/digital
ADC	analog to digital converter
CPU	central processing unit
DAC	digital to analog converter
DC, dc	direct current
DIP	dual inline package
EMI	electromagnetic interference
I/O	input/output
ICD	interface control document
IDAN	intelligent data acquisition node
ISA	industry standard architecture
ISS	*International Space Station*
LISN	line impedence simulation network
MSRR	materials science research rack

TECHNICAL MEMORANDUM

DEVELOPMENT OF ENHANCED AVIONICS FLIGHT HARDWARE SELECTION PROCESS

1. BACKGROUND

PC104 is an embedded systems specification that defines a miniature form factor for PC-compatible computers. Each board measures 3.55 by 3.775 in, and boards are stacked with 0.6-in clearance between them. The ISA bus is contained in a pair of self-stacking connectors (pins on bottom, socket on top), avoiding the need for a backplane. Boards are held together by standoffs in each corner. Also, the intelligent data acquisition node (IDAN) enclosures consist of modular, rugged, machined aluminum frames, and two coverplates held together by four shock-resistant fasteners (fig. 1). Each PC104 module has external I/O connectors accessible through its own frame. This allows the user to insert additional IDAN modules or restack the system at will. The goal of this research was to assemble a small data acquisition system (fig. 2) using different vendors of PC104 and test the system under different environments to see if it would qualify for flight, if any failures determine what needs to be modified to qualify it for flight.

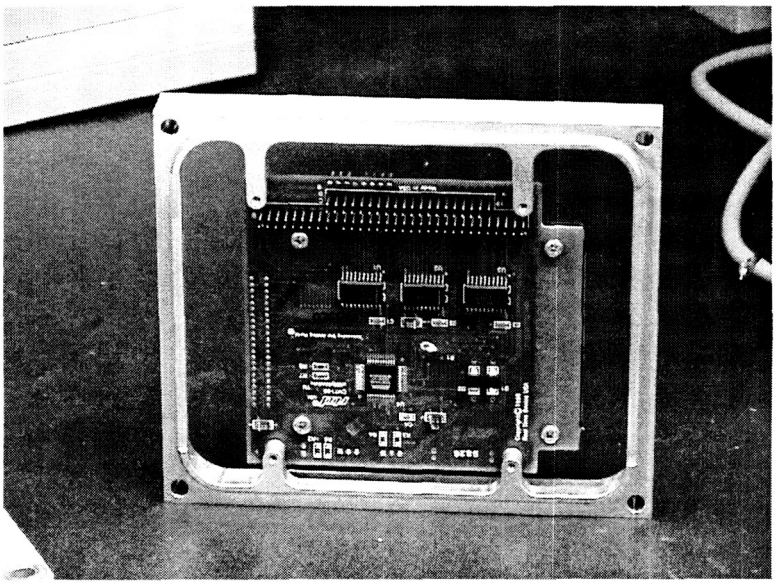

Figure 1. Hard drive module with aluminum frame.

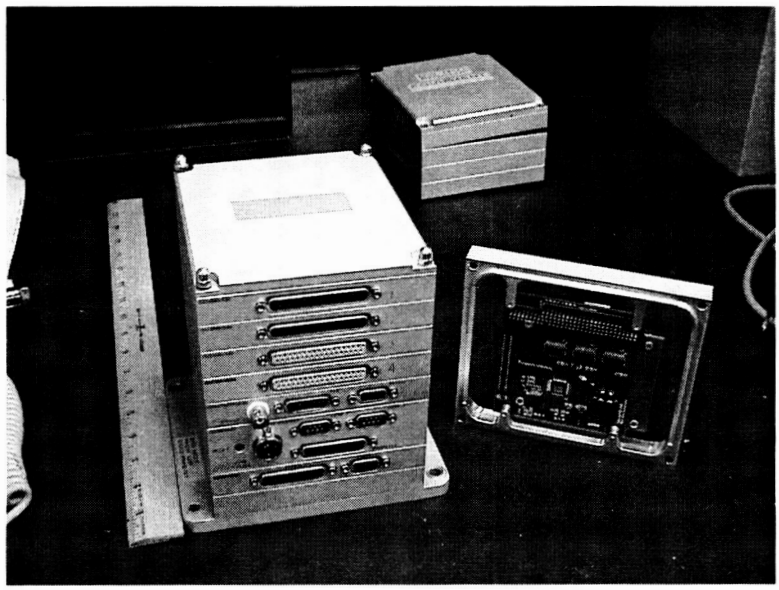

Figure 2. PC104-based data acquisition unit.

2. APPROACH

Our approach was to procure and build a functional small-scale data acquisition system (fig. 2). This system would perform the function of monitoring and collecting temperature sensor data and self-generated analog and discrete voltages. The first card in the stack was a high-efficiency ±5- and ±12-V power supply distributed by Tri-M Systems Inc. with an operating temperature range of –40 to 85 °C. The next card was a 16-MB 486DX cpuModule™ with two RS232/422/485 serial ports distributed by Real Time Devices with an operating temperature range of –40 to 85 °C. A 32-pin DIP, 144-MB DiskOnChip® was also used, distributed by M-Systems, with an operating temperature range of –40 to 85 °C to replace the hard drive in the test system. The next two cards were an 8-channel, 16-bit A/D resolution sensor module model 518 distributed by Sensoray with an operating temperature range of –25 to 85 °C. Two Arcom Control Systems AIM104–MULTI-IO cards complete the stack. Each card consists of a 16-channel, 12-bit ADC; a 2-channel, 12-bit DAC; and an 8-channel opto-isolated digital input. The temperature range of the AIM104–MULTI-IO cards is –20 to 70 °C. Each module is housed in the Real Time Devices IDAN aluminum frame (fig. 1).

3. ACCOMPLISHMENTS

3.1 Electromagnetic Interference Testing

The PC104 development unit underwent electromagnetic interference (EMI) susceptibility testing with the guidance of the E3 Team in the Environments Group (fig. 3). Since PC104 is a candidate for materials science research rack (MSRR) hardware, it was requested that testing be done to MSRR EMI requirements.

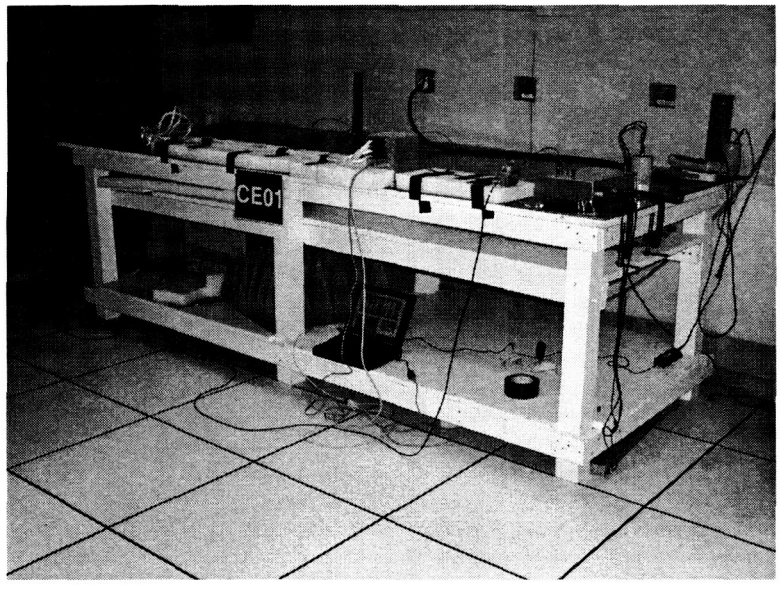

Figure 3. PC104 development unit prepared for EMI test.

The following EMI subtests were performed: CE01, CE03, RE02, RE04, DC Magnetic Field Emissions, CS01, CS02, CS06, RS02, and RS03. The CE07 test was not performed because the interface control documents (ICD) and SSP57000 documents specify that the line impedance simulation network (LISN) used for 120-V *International Space Station* (*ISS*) CE07 testing is to be used for MSRR–1 payloads using rack 28-V dc power. The *ISS* LISN simulates the *ISS* 120-V dc power bus impedance and is inappropriate for MSRR–1 28-V dc payload testing. The PC104 stack passed the CE01, CE03, RE04, DC Magnetic Field Emissions, CS01, CS06, and RS02 tests. PC104 failed the RE02 emissions test and revealed effects, as described in section 3.1.2, during the CS02 and RS03 susceptibility tests. Troubleshooting runs performed for both RE02 and RS03 indicated the need for cable shielding and PC104 stack shielding. Figure 4 shows PC104 stack shielding during RS03 troubleshooting.

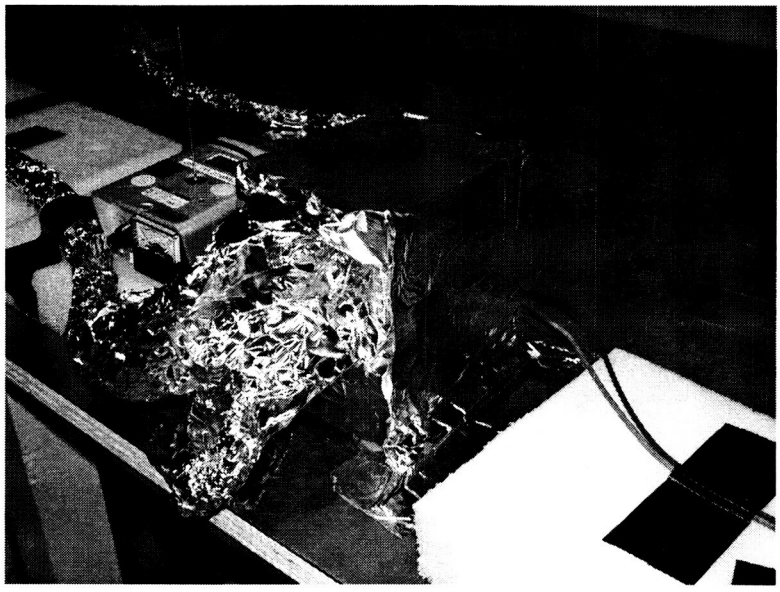

Figure 4. PC104 stack shielding during RS03 troubleshooting.

3.1.1 RE02

Overlimit emissions were observed as follows: a peak in the 14.4- to 21.3-kHz frequency range with a 1.6-dB maximum overlimit, 3.8 dB @ 1.585 MHz, 1.9 dB @ 1.945 MHz, 0.9 dB @ 2.035 MHz, 4.4 dB @ 11.1 MHz, 1.9 dB @ 11.3 MHz, a peak in the 14.3- to 16.7-MHz frequency range with a 4.4-dB maximum overlimit, 6.8 dB @ 58.05 MHz, 1.8 dB @ 260 MHz, 8.4 dB @ 268 MHz, 5.3 dB @ 276 MHz, 2.4 dB @ 284 MHz, 8.4 dB @ 300 MHz, 3 dB @ 308 MHz, 3.2 dB @ 316 MHz, 14 dB @ 332 MHz, 3dB @ 364 MHz, 0.9 dB @ 372 MHz, and 2.8 dB @ 500 MHz. Troubleshooting runs were performed to locate the sources of the overlimit emissions. The laptop computer and all cables were removed from the chamber; overlimit emissions in the 260- to 500-MHz range were reduced somewhat and all other overlimit emissions observed were reduced below the limit line. A new overlimit peak appeared in the 5.455- to 6.445-MHz frequency range with a 4.3-dB maximum overlimit. All data and signal cables were removed from the PC104: the 5.455- to 6.445-MHz peak disappeared, a new peak appeared in the 7.345- to 8.155-MHz frequency range with an 8.5-dB maximum overlimit, and the 260- to 500-MHz emissions increased slightly. The front of the PC104 stack was shielded with copper tape. The troubleshooting runs indicated the need for both shielded cables and shielding for the PC104 stack.

The CE07 test was not performed because the ICD and SSP57000 documents specify that the LISN used for 120-V *ISS* CE07 testing is to be used for MSRR–1 payloads using rack 28-V dc power. The *ISS* LISN simulates the *ISS* 120-V dc power bus impedance and is inappropriate for MSRR–1 28-V dc payload testing.

3.1.2 RS03

PC104 effects were observed in the 15-MHz to 2.8-GHz frequency range. The effects can be grouped into six categories: very slight thermocouple temperature variation (less than ±0.04 °C) as

observed on the laptop computer, thermocouple temperature variation (±0.1 °C) as observed on the laptop computer, thermocouple temperature readings on temperature board No. 2 going to all zeros as observed on the laptop computer, losing the RS232 communication link between the PC104 stack and the laptop computer, losing the Ethernet communication link between the PC104 stack and the laptop computer (which also "locked up" the laptop computer, requiring a reset), and "locking up" the PC104 processor card. The very slight thermocouple temperature variations were observed in the 15- to 30-MHz range at vertical polarization, near 200 MHz (both vertical and horizontal polarization), and 450-MHz to 1-GHz frequency range (horizontal polarization only). The thermocouple temperature variations were observed in the 400- to 450-MHz frequency range; temperature board No. 1 had greater variation than temperature board No. 2. The board No. 2 temperatures going to all zeros was only observed on one run in the 100- to 200-MHz frequency range at horizontal polarization and did not occur on any other runs. The RS232 communication link effects were only observed during the troubleshooting runs at 40.2 and 191.5 MHz. The Ethernet communication link effects were observed near 200 MHz in the initial runs for record. During troubleshooting runs, the Ethernet effects occurred at 42.2 MHz, 46.5 MHz, and in the 180- to 220-MHz range. The PC104 processor card "lockup" was only observed on one troubleshooting run near 42 MHz. Shielding all four cables between the PC104 stack and the thermocouple/discrete signal box significantly reduced the thermocouple temperature variation effect. Shielding the Ethernet cable, the PC104 stack, and all unused connectors on the PC104 stack eliminated the Ethernet link effects. The RS232 link effects were not investigated at the customer's direction. Thus, the RS03 troubleshooting indicated the need for both cable shielding and shielding of the PC104 stack.

The test was performed per MSRR–1 ICD–3–60078 and SSP57000 requirements using SSP30238 test methods. Full details of EMI testing are available in reference 1.

3.2 Electromagnetic Interference Recommendations

Preventing susceptibility to EMI is the primary focus of this section; doing so will prevent any electromagnetic noise from entering the system and help maintain a good operating balance. It is recommended to use a PC104 case that is solid and has the fewest openings and gaps as possible. Gaps that exist, such as small openings around electrical connectors, should be taped around with metal shielding to prevent EMI entering the case. In the event a solid box cannot be used, metal shielding should also be used around the gaps between the layers to electrically close off openings. Cabling should be adequately shielded as well; the shield should cover the length of the cable and be electrically connected to the PC104 case.

3.3 Vibration Testing

The PC104 development unit underwent random vibration excitation in each of its three axes for a duration of 3 min per axis at two separate levels. This was performed using a vibration table in building 4619 under the guidance of the Structural Dynamics/Vibroacoustics Group. These levels are as follows:

Level I:

20 Hz	@	0.01 g^2/Hz
20–80 Hz	@	3 dB/oct
80–350 Hz	@	0.04 g^2/Hz
350–2,000 Hz	@	–3.0 dB/oct
2,000 Hz	@	0.007 g^2/Hz
		Composite = 6.1 g

Level II:

20 Hz	@	0.04 g^2/Hz
20–80 Hz	@	3 dB/oct
80–350 Hz	@	0.16 g^2/Hz
350–2,000 Hz	@	–3.0 dB/oct
2,000 Hz	@	0.028 g^2/Hz
		Composite = 12.1 g

The test plan for the implementation of the level I test is as follows:

(1) Perform functionality test of PC104.
(2) Perform sine sweep of PC104 at 0.25g from 5 to 2,000 Hz at a rate of 2 oct/min.
(3) Perform random vibration test in one axis.
(4) Perform sine sweep.
(5) Perform functionality test.
(6) Repeat steps 2 through 5 for other two axes.

The test plan for the implementation of the level II test is as follows:

(1) Perform random vibration test in one axis.
(2) Perform sine sweep.
(3) Perform functionality test.
(4) Repeat steps for other two axes.

The PC104 development unit was placed on a shaker table with instrumentation necessary for the test engineer to conduct vibration and shock testing (fig. 5).

The sine sweep tests were complete for both levels. Level I random tests were complete in the *X*-*Y*-*Z* axes but level II random tests were run in the *Z* axis only. An anomaly was discovered after the level II *Z*-axis test and the test was stopped. Inspection of the boards revealed the battery was shaken completely off as well as several ribbon connectors on the CPU board, preventing the unit from functioning. Full details of vibration testing are available in reference 2.

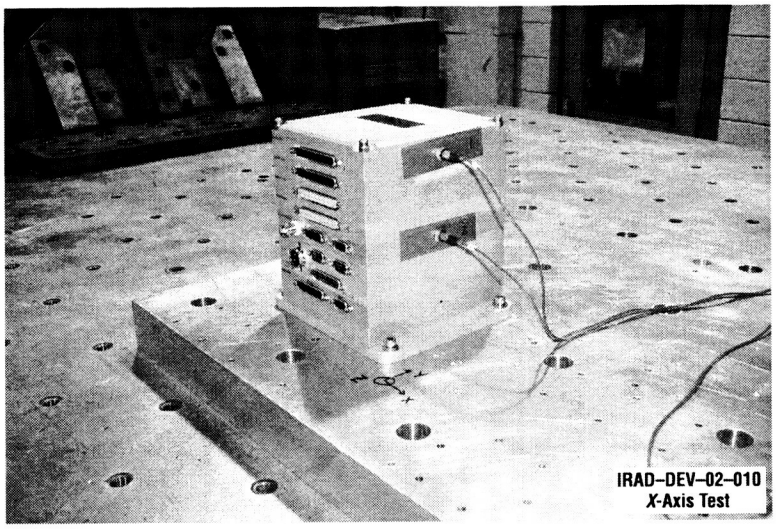

Figure 5. PC104 unit prepared for vibration test.

3.4 Vibration Recommendations

It is recommended that staking all loose parts consisting of jumpers, connectors, batteries, and board to chassis screws will solve this problem.

3.5 Thermal Cycle Testing

Thermal cycle testing was performed to find out what temperature ranges the PC104 hardware could withstand without any modifications. This was performed using a thermal cycle chamber in building 4612 under the guidance of the Thermal and Fluid Systems Group. The chamber was controlled to a low humidity level to prevent condensation at low temperatures. All of the hardware was contained in the thermal chamber during thermal cycling (fig. 6).

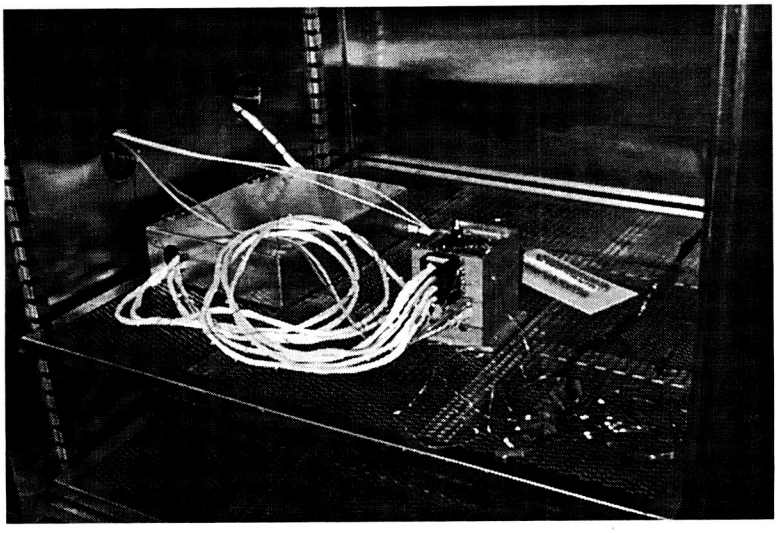

Figure 6. PC104 unit prepared for thermal cycle test.

Five thermocouples were inserted into the PC104 stack to measure temperatures of key components of the system: CPU board, DiskOnChip module, Ethernet board, one Sensoray board, and one Arcom board. The chamber was then cycled to the following temperatures and held until the temperature readings of all the measured components reached desired levels and were properly soaked: –20 °C, 30 °C, –30 °C, 40 °C, –40 °C, 50 °C, –40 °C, and 60 °C.

After each desired temperature had been thoroughly soaked, a functional test was performed on the PC104 hardware. The functional tests consisted of powering on the PC104 stack, running the software on the host notebook computer, and verifying correct communication between the host computer and the PC104 stack. The software was then set to record data for ≈5 min at each level.

At each of the low temperatures, extended time of testing was not a high priority. Once verification of correct hardware performance was determined, the PC104 stack began to warm up under its own power. However, extended testing was a necessary issue at higher temperatures. The PC104 stack will always increase in temperature above the environment it is exposed to. Once 60 °C was reached, the PC104 stack was left on while measured temperatures were observed. When the CPU card temperature measurement reached ≈67 °C, the hardware failed. The chamber temperature was lowered to 50 °C to perform a second test. The hardware successfully began operation again; however, it failed and stopped responding again when the measured CPU temperature reached 67 °C. All other temperatures were well below their previous readings from the 60 °C test. The CPU module was determined to be the weak component in the system at high temperatures.

3.6 Thermal Cycle Recommendations

The following are recommendations based on thermal cycle testing results:

- A shirtsleeve environment is recommended for PC104 in its off-the-shelf configuration.
- Active cooling is needed for this PC104 hardware when exposed to high temperatures.
- An interface material (cotherm) between the cards will improve heat conduction between stacks.
- Locate hot chips at ambient and have a frame machined with a heat sink on hot spots to achieve cooler component temperatures.
- An aluminum plane mounted to the module sidewalls and bonded to the high dissipation board components would be another option.
- Work with Real Time Devices on a custom-designed, environmentally sealed enclosure.

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1. Shelby, G.A.; PC104 IRAD EMI Test Report, *CA01–EMI–027*, Marshall Space Flight Center, AL, September 28, 2001.

2. Brewster, S.; PC104 Development Unit Vibration Test Report, TCP No. *IRAD–DEV–01–108*, Marshall Space Flight Center, AL, May 14, 2002.

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13. ABSTRACT *(Maximum 200 words)*

The primary objective of this research was to determine the processes and feasibility of using commercial off-the-shelf PC104 hardware for flight applications. This would lead to a faster, better, and cheaper approach to low-budget programs as opposed to the design, procurement, and fabrication of space flight hardware. This effort will provide experimental evaluation with results of flight environmental testing. Also, a method and/or suggestion used to bring test hardware up to flight standards will be given. Several microgravity programs, such as the Equiaxed Dendritic Solidification Experiment, Self-Diffusion in Liquid Elements, and various other programs, are interested in PC104 environmental testing to establish the limits of this technology.

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